

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 2001351976 A

(43) Date of publication of application: 21.12.01

(51) Int. Cl

**H01L 21/768**  
**H01L 21/28**  
**H01L 21/316**  
**H01L 21/3205**

(21) Application number: 2001117668

(22) Date of filing: 17.04.01

(30) Priority: 17.04.00 US 2000 550943

(71) Applicant: INTERNATL BUSINESS MACH CORP <IBM>

(72) Inventor: DALTON TIMOTHY J  
CHRISTOPHER V JARNES  
JOYCE C RYUU  
PURUSHOTHAMAN SAMPATH

**(54) METHOD FOR PROTECTING LOW-PERMITTIVITY LAYER ON SEMICONDUCTOR MATERIAL**

permittivity, before the interconnection structure of the inter-level dielectric is formed.

COPYRIGHT: (C)2001,JPO

(57) Abstract:

**PROBLEM TO BE SOLVED:** To provide a permanent protection hard mask for protecting the dielectric characteristics of a main dielectric layer that has undesired low permittivity of a semiconductor device due to undesired increase in permittivity, undesired increase in current leakage, and a low device yield caused by surface scratch, when a continuous treatment processing is conducted.

**SOLUTION:** This protection hard mask has a one- or two-layer sacrificial hard mask that is especially effective, when interconnection structure such as a via opening and/or a line is formed between low-permittivity materials, while a final product is manufacture. The sacrificial and permanent hard masks are formed of the same precursor substance in a single process, where process conditions are changed for giving a film having different permittivity. Most preferably, dual damascene structure has three-layer hard masks 40, 50, and 60 that are formed on the inter-level dielectric with bulk low

